A DVS sensor with a Photovoltaic Receptor

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***Abstract*—Dynamic Vision Sensors (DVS) face limitations due to noise-power trade-offs, pixel pitch constraints, and readout inefficiencies. This work presents the Photovoltaic Dynamic Vision Sensor (PVDVS), which replaces the conventional photoreceptor with a single photovoltaic diode. Its self-biasing nature removes the dependence of the static power on illumination, and the noise power reaches diode's shot noise limit without additional consumption. PVDVS also achieves a wider dynamic range, higher SNR, and enhanced contrast sensitivity across a broad illuminance range, making it a strong candidate for next-generation event-based vision sensors.**

***Index Terms*—DVS sensor, photovoltaic, diode, solar cell, AER, event-based, vision sensor, asynchronous.**

I. Introduction

Dynamic Vision Sensors (DVS) have gained significant industrial interest, with major companies such as Samsung, Sony, and Omnivision integrating them into their sensor portfolios [1]–[3]. However, challenges such as noise-power trade-offs, pixel pitch constraints, and readout inefficiencies limit their full potential [4].

Pixel pitch reduction has been a major focus, as early DVS implementations required large pixel sizes to accommodate complex circuitry [5]. Although vertical integration has allowed for pixel scaling below 5 µm [6], these technologies remain costly, highlighting the need for alternative approaches. Additionally, power consumption and latency must be minimized as pixel counts increase, but most DVS pixels still adhere to the original 2008 design [7], restricting opportunities for efficiency improvements.

Noise performance is critical and has an impact on temporal contrast sensitivity, dynamic range, and background activity noise. Motion artifacts and background activity noise from pixels, which strongly depend on illumination and photoreceptor biasing [8], further degrade performance in low-light conditions. Existing solutions introduce additional circuitry [1], [3], increasing complexity and power consumption.

This work proposes an alternative pixel front-end: the Photovoltaic Dynamic Vision Sensor (PVDVS) [9], which replaces the conventional reverse-biased photoreceptor with a self-biased photovoltaic diode. PVDVS offers advantages in pixel size reduction, noise performance, and power efficiency. We present its experimental characterization, demonstrate its suitability for temporal contrast detection, and discuss its advantages and limitations based on theoretical modeling and experimental results.

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II. Implementation of a Photovoltaic DVS

A. Diode in Photovoltaic Regime

As illustrated in Fig. 1**a**, the voltage (V_D) between anode and cathode of a diode operating in the photovoltaic regime exhibits a logarithmic dependence on illuminance. The current across the junction, $I_D = I_{GR} - I_{DIFF}$, consists of two components: one related to generation-recombination processes, I_{GR}, and the other due to the diffusion current, I_{DIFF}.

In the photovoltaic regime, the maximum attainable voltage is the open-circuit voltage, V_{oc}, corresponding to the diode voltage when no current flows through its terminals. If the anode is connected to a high-impedance node, V_D will tend toward V_{oc}. Its value depends on the illumination level, as follows:

$$V_{oc} = \eta U_T \ln\left(1 + \frac{I_{GR}}{I_S}\right) \approx \eta U_T \ln\left(1 + \frac{I_{ph}}{I_S}\right) \quad (1)$$

where I_{ph} is the photocurrent and I_S is the diode's specific current. Hence, in terms of temporal contrast detection, the PVDVS operation is equivalent to that of a conventional DVS, as the photovoltaic diode in an open-circuit configuration provides an output voltage proportional to the logarithm of the photocurrent [10].

B. Pixel Architecture

Fig. 1**b** depicts the pixel architecture. The conventional photologarithmic receptor has been replaced with a diode operating in the photovoltaic regime, performing both photodetection and logarithmic compression within a single device. The subsequent stages remain the same as those proposed in the original DVS implementation [7], that is, a source follower to isolate the photoreceptor from the amplification stage, a differencing amplifier, comparators and in-pixel logic.

A PMOS source follower has been designed to match the linear region within the range of $[0, 500]$ mV, which corresponds to typical V_{oc} values for CMOS-integrated diodes under standard illumination conditions [10]. The change amplifier primarily determines the pixel gain and is given by the ratio of capacitances, $C_1/C_2 \approx 19$. The two-stage OTA comparators were not optimized for area consumption to prioritize achieving higher resolution in the comparator stage.

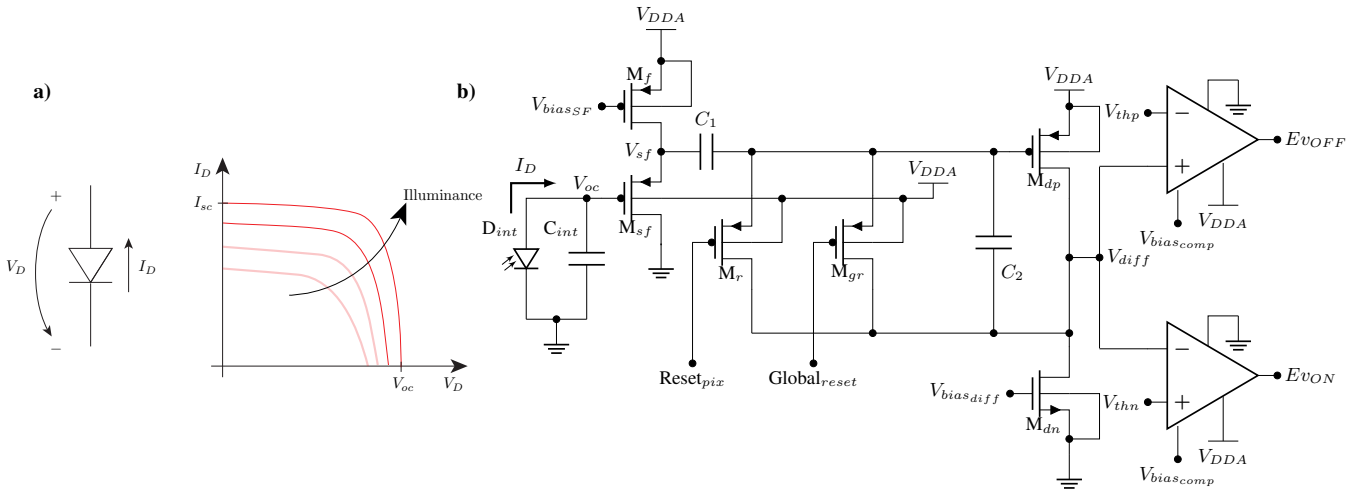

Fig. 1. (**a**) Diode IV characteristics in the photovoltaic regime. (**b**) The pixel core schematic, designed by the authors, replaces the classic logarithmic photoreceptor front-end stage with a single diode operating in the photovoltaic regime. Transistors' dimensions W/L $\left(\frac{\mu m}{\mu m}\right)$ and capacitance values are as follows: M$_{sf}$, M$_f$: 0.6/0.6, M$_r$, M$_{gr}$: 0.24/0.18, M$_{dp}$: 0.9/1, M$_{dn}$: 0.6/2, $C_1 = 122$ fF, $C_2 = 6.5$, fF.

III. Theory and Experimental Characterization

A 64×96-pixel test chip prototype was fabricated using UMC's 180nm technology. A microphotograph of the chip is shown in Fig. 2. This section presents and discusses the experimental results, validating our theoretical model, and providing a deeper understanding of this approach.

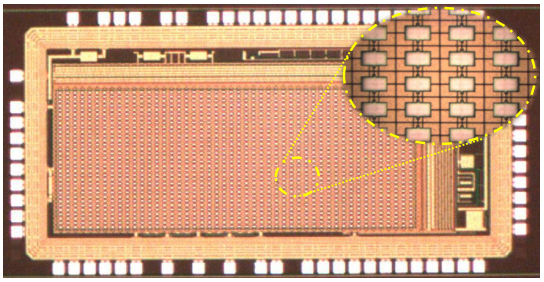

Fig. 2. Chip Microphotograph including a pixel-scale photo. Pixel dimensions are 12.4 µm × 21.5 µm.

A. Noise Performance

With this architecture, the noise power is reduced to the fundamental limit of 2× photon shot noise, $4qI_{ph}$, without additional power consumption [8]. Because the diode is forward self-biased, the load capacitance is determined by its junction or diffusion intrinsic capacitance at low and high illuminance, respectively. This leads to reduced integrated noise, kT/C [11], at the cost of limiting the sensor's bandwidth. These factors combine to significantly reduce noise events [9].

1) Power Noise of the Photovoltaic Receptor: The Power Spectral Density (PSD) was measured with a Spectrum Analyzer and subsequently integrated to obtain the RMS voltage. This measurement was repeated under varying illuminance and temperature conditions using neutral filters and a heat pistol, respectively. The results are shown in Fig. 3**a**. The V_{rms}

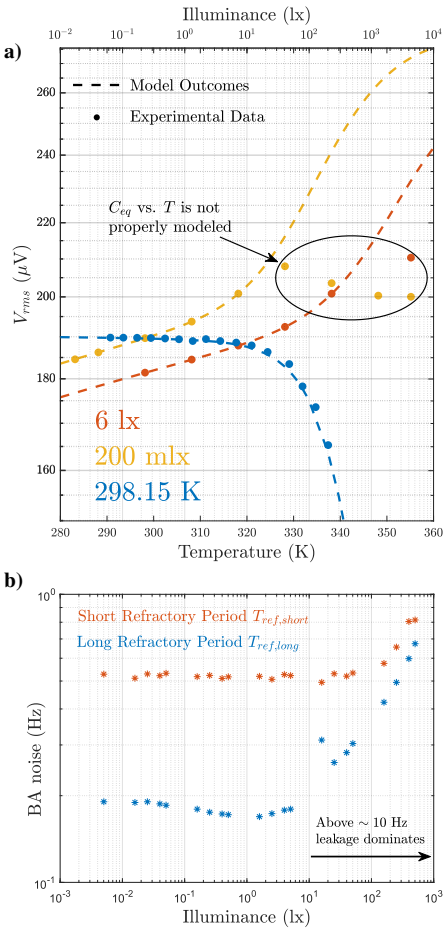

Fig. 3. Noise performance of the PVDVS. (**a**) Model outcomes and experimental data of the diode's RMS noise voltage vs. illuminance at room temperature, $T_{room} = 298.15$ K, and vs. temperature for two different illumination levels. (**b**) Noise event rate for different bias settings.

exhibits a peak of $\sim$ 210 µV at low illuminance and high temperature values. It remains lower than previously reported RMS values for the logarithmic photoreceptor, even under optimal biasing or with a reduced integration bandwidth [8].

2) Background Activity Noise: In the classic architecture, the main noise sources contributing to generating undesired events at low illuminance are the photoreceptor stage's Shot and Thermal noise, while at bright scenes it will be the leakage current in the change detector [3], [8]. In our case, as shown in Fig. 3**b**, the Background Activity noise is constant for dim scenes. As illuminance increases, the leakage current becomes important, increasing BA noise, above $\sim$ 10 lx. Longer refractory periods reduce BA noise.

B. Temporal Contrast Sensitivity

Previous works [7], [12] defined temporal contrast as $\ln\left(I_{ph_{max}}/I_{ph_{min}}\right)$, where $I_{ph_{max}}$ and $I_{ph_{min}}$ are the maximum and minimum photocurrents corresponding to high and low stimulus states, respectively.

For the proposed pixel architecture, considering that the open-circuit voltage follows (1), the temporal contrast is proportional to the transient variation of the open-circuit voltage:

$$TC = \frac{\partial I_{ph}}{\partial t}\frac{1}{I_{ph}} = \frac{\partial \ln\left(I_{ph}\right)}{\partial t} \approx \frac{\partial V_{oc}}{\partial t}\frac{1}{\eta U_T} \approx \frac{\Delta V_{oc}}{\eta U_T} \quad (2)$$

Thus, the threshold temporal contrast is defined as:

$$\theta_{\text{ON/OFF}} = \Delta V_{oc}|_{\text{ON/OFF}} = \frac{C_2}{C_1 \kappa_{SF}}\left(V_{rst} - V_{thi}\right) \quad (3)$$

where $i = n, p$ for ON/OFF temporal contrast, respectively. The rate of generated ON/OFF events is then given by:

$$\text{Event Rate } (t) = \frac{1}{\eta U_T \theta_{\text{ON/OFF}}}\frac{\partial V_{oc}}{\partial t} \quad (4)$$

However, this estimation is affected by the sensor's noise performance. Fig. 4**a** illustrates the sensor diode response for the temporal contrasts 10% and 40% as a function of illuminance. Both remain constant until the dark current becomes significant compared to the signal, limiting temporal contrast sensitivity at low illuminance due to SNR degradation. Consequently, the Uniformity of Response (UoR) deteriorates in dim scenes. Furthermore, since ΔV_{oc} remains constant in bright scenes, the upper limit of the TC sensitivity is constrained by leakage in the Change Amplifier. As a result, this strategy allows contrast sensitivity down to 1% within an illuminance range of $[50, 500]$ mlx, reaching the limits at $\sim$ 5 mlx and $\sim$ 10 lx, where the sensitivity increases to 30% and 10%, respectively. This approach provides high contrast sensitivity across a broader illuminance range. Since the gain is governed by the thermal voltage, the system achieves 1% TC sensitivity due to the higher resolution of the comparator stage, which also improves latency.

C. Dynamic Range

Fig. 4**b** shows the probability of detection of pixels for two temporal contrast values (10 and 30%). PVDVS achieves a wider dynamic range due to its self-biased operation, which mitigates the effects of transistor leakage and results in a higher SNR. It operates efficiently to 30 mlx for a temporal contrast of 10% and $\sim$ 5 mlx for a contrast of 30%. This range could be extended for higher temporal contrasts, as the lower limit is determined by the signal-to-noise ratio. The upper limit is set by the photogenerated leakage current in the differentiator stage, reaching 3 klx for a temporal contrast of 10% and 24 klx for a contrast of 30%.

D. Power Consumption

Fig. 5 illustrates the sensor's power consumption. While dynamic power consumption increases with the event rate as expected, the static power consumption remains independent of illuminance, an important feature of this topology because the proposed photoreceptor stage is self-biased.

E. State-of-The-Art Comparison

Beyond supporting expectations for potential advantages in area and power consumption, due to the simplicity of the photovoltaic receptor and its self-biased property, Table I demonstrates that PVDVS achieves compelling results in terms of contrast sensitivity, dynamic range, latency, and noise performance. The metrics highlight significant advantages in low-illumination conditions, particularly in terms of noise performance and contrast sensitivity for high dynamic range operation. Notably, this performance is achieved without requiring preamplification or a high-gain differencing amplifier, and crucially, without a power-noise trade-off. This further benefits pixel background activity noise and latency.

TABLE I
STATE-OF-THE-ART COMPARISON

	This work	iniVation DAVIS346 [13]	OmniVision 2023 [2]	PROPHESEE 2020 [6]
Technology	0.18 µm 1P6M UMC	0.18 µm 1P6M MIM CIS	40 nm BSI-CIS +65 nm CMOS +3DMIM +40 nm CMOS	90 nm BI-CIS +40 nm CMOS
Supply Voltage (V)	1.8	1.8	–	2.5, 1.1
Resolution	64 × 96	346 × 260	1032 × 928	1280 × 720
Pixel size (µm^2)	12.45 × 21.5*	18.5 × 18.5	8.8 × 8.8	4.86 × 4.86
Fill Factor	18%	22%	1/16	> 77%
Power/Pixel (nW)	410*	–	31	35
Max event rate (Meps)	10.64	12	4600	1066
Contrast Sensitivity	**1% (0.05 − 0.5** lx) **10% (0.5 − 500** lx)	14.3% (ON) 22.5% (OFF)	15% (10 − 1000 lx)	11%
CTNU	5% (> 15 lx)	3.5%	3% (> 10 lx)	3%
Dynamic Range (dB)	**100 (10%** TC) **> 140 (30%** TC)	120	–	> 124 (40% TC)
Latency +/− (µs)	**3.7/7.6@500 lx 200/267@5 lx 2180/2380@50 mlx**	< 1000	200@100 lx 100@1 klx	–
Peak Noise Activity (Hz)	**< 1**	1 (I_{pr} = 2 pA) 100 (I_{pr} = 50 pA)	< 1	8.3
V_{rms} (mV)	**0.19 (< 1 lx, T$_{\text{room}}$) 0.21 (High T) @Δf ∼ 100 kHz**	1.7 (I_{pr} = 2 pA) 2.4 (I_{pr} = 50 pA) (< 1 lx) @Δf ∼ 4 kHz	–	–

* Pixel pitch and power consumption could be reduced by optimizing the building block topologies.

F. Sample Images

The sensor's operation is demonstrated in Fig. 6, which shows its response under various stimuli and illumination levels, confirming a contrast sensitivity exceeding 10% (Edmund chart test). The characteristic intra-scene dynamic range of the DVS is illustrated in a visual scene where the Edmund chart moves across two regions with significantly different illumination levels. At low illuminance, slight image blurring occurs as a result of increased sensor latency.

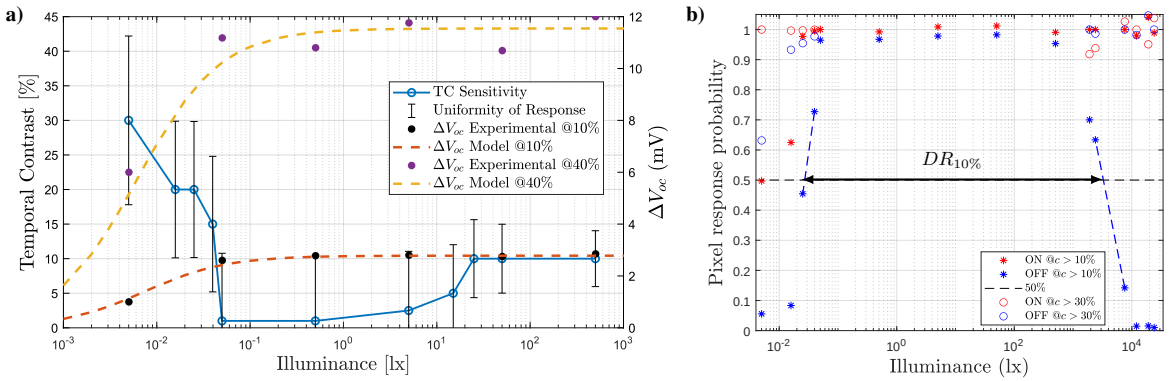

Fig. 4. (**a**) Minimum detectable temporal contrast and diode's open-circuit voltage sensitivity vs. illuminance for two contrasts: $c = 10\%$ and 40%. (**b**) PVDVS's dynamic range for two contrasts: $c = 10\%$ and 30%.

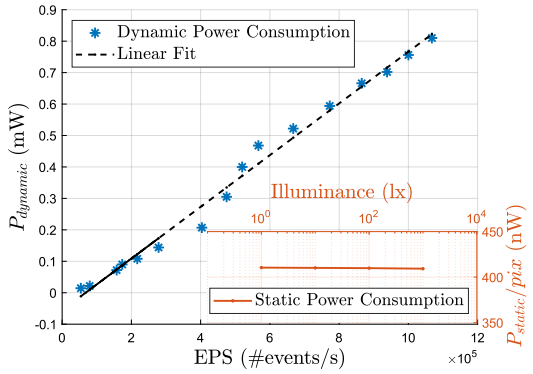

Fig. 5. The entire sensor's dynamic power consumption as a function of the event rate is shown, along with a single pixel static power consumption versus illuminance in the bottom-right corner.

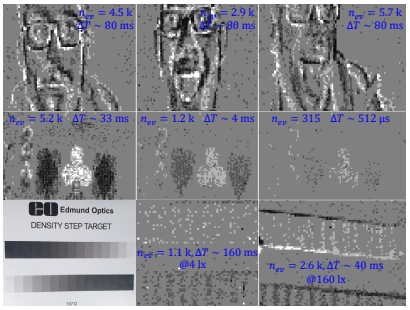

Fig. 6. Sample images acquired with the sensor: faces, cards moving at high speed, snapshots of the Edmund chart, and letters moving within scenes with large intra-dynamic range.

IV. Conclusion

A DVS sensor prototype based on an alternative pixel architecture has been presented and characterized experimentally. The main achievement of this work is to demonstrate that the classic front-end photoreceptor stage of DVS pixels can be substituted by a diode operating in the photovoltaic regime. The proposed architecture considerably improves latency and noise performance, has higher sensitivity with low illumination, and potentially reduces area and power consumption.

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